**AIC HW1**

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# Code for Problem 1 & 2

1. \*\*\*-----------------------\*\*\*

2. \*\*\*        setting        \*\*\*

3. \*\*\*-----------------------\*\*\*

4. .lib "~/U18\_HSPICE\_Model/mm180\_reg18\_v124.lib" ff

5. .TEMP 25

6. .op

7. \*\*\*-----------------------\*\*\*

8. \*\*\*       simulation      \*\*\*

9. \*\*\*-----------------------\*\*\*

10. .option post

11. .tran 0.1n 60n

12.

13. .DC V1 0V 1.8V 1mV

14. .probe id\_mos = I(MN)

15. \*\*\*-----------------------\*\*\*

16. \*\*\*      parameters       \*\*\*

17. \*\*\*-----------------------\*\*\*

18. .param wn = 5.4u

19. .param ln = 1.8u

20. .global VDD GND

21. \*\*\*-----------------------\*\*\*

22. \*\*\*      power/input      \*\*\*

23. \*\*\*-----------------------\*\*\*

24. Vsupply VDD GND 1.8v

25. V1 Vds GND 1.8V

26. V2 Vgs GND 1.8V

27. \*\*\*-----------------------\*\*\*

28. \*\*\*        circuit        \*\*\*

29. \*\*\*-----------------------\*\*\*

30. MN  Vds VDD GND GND n\_18\_mm w=wn l=ln

31.

32. \*\*\*-----------------------\*\*\*

33. \*\*\*         alter         \*\*\*

34. \*\*\*-----------------------\*\*\*

35. .alter

36. .param wn = 0.54u

37. .param ln = 0.18u

38. .end

# Problem 1

According to the waveforms and simulated values, is smaller in the SS corner, and larger in the FF corner when compared to TT. The following is the meaning of each corner:

SS (Slow-Slow) Corner: Both NMOS and PMOS transistors are slow. The MOSFETs have higher threshold voltages. The circuit operates slower in this corner. It represents a worst-case scenario in terms of performance.

TT (Typical-Typical) Corner: Both NMOS and PMOS transistors exhibit typical behavior. The process variation is minimal, and the transistor characteristics match the nominal or average conditions.It is the reference point when comparing performance under other corners like SS (slow) or FF (fast).

FF (Fast-Fast) Corner: Both NMOS and PMOS transistors are fast. This results in lower threshold voltages and faster switching, causing the circuit to operate more quickly. It represents a best-case scenario in terms of performance.

|  |  |
| --- | --- |
| Corner | @ = = 1.8V  W/L=5.4um/1.8um |
| TT | 一張含有 文字, 行, 繪圖, 圖表 的圖片  自動產生的描述 |
| SS | 一張含有 文字, 行, 繪圖, 圖表 的圖片  自動產生的描述 |
| FF | 一張含有 文字, 行, 繪圖, 圖表 的圖片  自動產生的描述 |

|  |  |
| --- | --- |
| Corner | @ = = 1.8V  W/L=0.54um/0.18um |
| TT | 一張含有 文字, 行, 繪圖, 圖表 的圖片  自動產生的描述 |
| SS | 一張含有 文字, 行, 繪圖, 圖表 的圖片  自動產生的描述 |
| FF | 一張含有 文字, 行, 繪圖, 圖表 的圖片  自動產生的描述 |

# Problem 2

The simulated values are smaller than calculated values potentially due to second-order effects like mobility degradation and narrow-width effect:

**Mobility Degradation:**

The effective mobility of charge carriers degrades with higher electric fields (especially in short-channel devices). In my hand calculations, I assume that is constant, whereas HSPICE uses more realistic models that account for mobility degradation under strong inversion conditions.

**Narrow-Width Effect:**

When the width of the transistor becomes very small (narrow-width devices), the fringing fields from the gate extend into the sidewalls, causing more of the substrate to be depleted. This makes it harder for the gate to invert the channel, effectively increasing . Notice that even though W/L=5.4um/1.8um & W/L=0.54um/0.18um have the same ratio, is smaller when W/L=0.54um/0.18um.

|  |  |  |
| --- | --- | --- |
| Param. | Sim. | Cal. |
| W/L=5.4um/1.8um |  |  |
| W/L=5.4um/1.8um |  |  |
| W/L=0.54um/0.18um |  |  |
| W/L=0.54um/0.18um |  |  |

# Code for Problem 3

1. \*\*\*-----------------------\*\*\*

2. \*\*\*        setting        \*\*\*

3. \*\*\*-----------------------\*\*\*

4. .lib "~/U18\_HSPICE\_Model/mm180\_reg18\_v124.lib" tt

5. .TEMP 25

6. .op

7. \*\*\*-----------------------\*\*\*

8. \*\*\*       simulation      \*\*\*

9. \*\*\*-----------------------\*\*\*

10. .option post

11. .DC V1  0V 1.8V 1mV sweep V2  0V 1.8V 0.2V

12. .probe id\_mos = I(MN)

13.

14. \*\*\*-----------------------\*\*\*

15. \*\*\*      parameters       \*\*\*

16. \*\*\*-----------------------\*\*\*

17. .param wn = 5.4u

18. .param ln = 1.8u

19. .param ls = 0.48u

20. .global VDD GND

21.

22. \*\*\*-----------------------\*\*\*

23. \*\*\*      power/input      \*\*\*

24. \*\*\*-----------------------\*\*\*

25. Vsupply VDD GND 1.8v

26. V1 Vds GND 1.8V

27. V2 Vgs GND 1.8V

28. \*\*\*-----------------------\*\*\*

29. \*\*\*        circuit        \*\*\*

30. \*\*\*-----------------------\*\*\*

31. MN  Vds Vgs GND GND n\_18\_mm w=wn l=ln AD = 'ls \* wn' AS = 'ls \* wn' PD = '2\*ls + wn' PS = '2\*ls + wn'

32.

33. \*\*\*-----------------------\*\*\*

34. \*\*\*         alter         \*\*\*

35. \*\*\*-----------------------\*\*\*

36. .alter

37. .param wn = 0.54u

38. .param ln = 0.18u

39.

40. .end

# 一張含有 文字, 行, 繪圖, 圖表 的圖片 自動產生的描述Problem 3

一張含有 行, 繪圖, 文字, 平行 的圖片

自動產生的描述Fig 1. W/L=0.54/0.18um IV Curve (with perimeter)

Fig 2. W/L=0.54/0.18um IV Curve (without perimeter)

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自動產生的描述 Fig 3. MOSFET Characteristics (left: without perimeter / right: with perimeter)

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自動產生的描述

一張含有 行, 繪圖, 文字, 圖表 的圖片

自動產生的描述

Fig 4. W/L=5.4/1.8um IV Curve (without perimeter)

**Channel length modulation:**

At high ​, the depletion region near the drain widens, causing the channel to "pinch off" near the drain. If we increase even further, the pinch off point moves closer to the source. This shortens the channel length, allowing more current to go through. In this case, becomes dependent on , so we modify the original equation by introducing a *(1+λ)* term.

(*λ* is the channel length modulation parameter)

This should make the simulated current higher than my hand calculation, which ignored channel length modulation. However, as observed in problem 2, this is not the case. I think it might be that there are other second-order effects present, further complicating things.

**Velocity saturation:**

When the drift velocity of charge carriers (electrons or holes) in the transistor channel reaches a maximum limit, despite further increases in the applied electric field. This occurs because at high electric fields, the carrier velocity no longer increases linearly with the field but instead saturates due to scattering effects. In short-channel MOSFETs, velocity saturation becomes significant. The current in the transistor becomes less sensitive to the gate voltage because increasing the field further does not increase the carrier velocity significantly. Notice that even though W/L=5.4um/1.8um & W/L=0.54um/0.18um have the same ratio, increases more with when L = 1.8um.

**What difference with specifying the area & perimeter make?**

The current values in fig 1 & 2 look identical. It doesn’t seem like adding area & perimeter to the simulation affected current. However, the parasitic capacitance was reduced after specifying the perimeter. This shows that parameters (area and perimeter) are essential for accurately modeling the parasitic capacitances and resistances in MOSFETs.